CLAIMS

What is claimed is:

1. A system comprising:

a direct memory access (DMA) controller; and

an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller is adaptable to terminate a DMA transfer before a terminal count is reached.

2. The system of claim 1 wherein the DMA controller is adaptable to re-execute a DMA transfer with the I/O device.

3. The system of claim 1 wherein the DMA controller is adaptable to operate in a normal mode and a descriptor mode

4. The system of claim 3 wherein the DMA controller executes a series of single transfers to the I/O device while operating in the descriptor mode.

5. The system of claim 4 wherein the DMA controller is adaptable to automatically determine the sequence of the single transfers to be performed while operating in the descriptor mode.

6. The system of claim 1 further comprising:

a system interconnect coupled to the I/O device and the DMA controller;

a central processing unit (CPU) coupled to the system interconnect; and

a memory device coupled to the system interconnect.

7. The system of claim 1 wherein the DMA controller comprises:

one or more DMA channels; and

a configuration register matrix coupled to one or more DMA channels.

8. The system of claim 7 wherein each of the DMA channels comprises:

control logic; and

descriptor logic.

9. A system comprising:

a direct memory access (DMA) controller; and

an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller is adaptable to operate in a normal mode and a descriptor mode.

10. The system of claim 9 wherein the DMA controller is adaptable to re-execute a DMA transfer with the I/O device.

11. The system of claim 9 wherein the DMA controller is adaptable to terminate a DMA transfer to or from the I/O device.

12. A system comprising:

a direct memory access (DMA) controller; and

an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller is adaptable to re-execute a DMA transfer with the I/O device.

13. A method comprising:

transferring data between a first device and a second device under control of a direct memory access (DMA) controller;

receiving a request signal at the DMA controller from the first device, wherein the request signal indicates a request by the first device to re-transmit the data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device; and

re-transferring the data between the first device and the second device.

14. The method of claim 13 further comprising reloading configuration registers within the DMA controller prior to transmitting the acknowledge signal to the first device.

15. A method comprising:

transferring data between a first device and a second device under control of a direct memory access (DMA) controller;

receiving a request signal at the DMA controller from the first device, wherein the request signal indicates a request by the first device to terminate the transfer of data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device; and

terminating the transfer of data between the first device and the second device.

16. The method of claim 13 further comprising clearing a counter within the DMA controller prior to transmitting the acknowledge signal to the first device.

17. A method of executing a direct memory access (DMA) transfer comprising:

retrieving a first set of commands from a descriptor table at a DMA controller;

receiving a first request signal at the DMA controller from the first device, wherein the request signal indicates a request by the first device to transfer data between the first device and a second device under the control of the DMA controller;

transmitting a first acknowledge signal from the DMA controller to the first device; and

transferring data between the first device and the second device according to the first set of commands.

18. The method of claim 17 further comprising constructing the descriptor table within a memory device.

19. The method of claim 17 further comprising programming the first set of commands in to configuration registers within the DMA controller after retrieving the first set of commands.

20. The method of claim 17 further comprising:

determining whether more commands are stored in the descriptor table; if so,

retrieving a second set of commands from the descriptor table;

receiving a second request signal at the DMA controller from the first device;

transmitting a second acknowledge signal from the DMA controller to the first device; and

transferring data between the first device and the second device according to the second set of commands.

21. The method of claim 17 further comprising:

receiving a second request signal at the DMA controller from the first device, wherein the second request signal indicates a request by the first device to re-transmit the data between the first device and the second device;

transmitting a second acknowledge signal from the DMA controller to the first device; and

re-transferring the data between the first device and the second device according to the first set of commands.

22. The method of claim 17 further comprising:

receiving a second request signal at the DMA controller from the first device, wherein the second request signal indicates a request by the first device to terminate the data between the first device and the second device;

transmitting a second acknowledge signal from the DMA controller to the first device; and

terminating the transfer of data between the first device and the second device.

23. The method of claim 22 further comprising:

reducing a transfer count within the descriptor table after terminating the transfer; and

retrieving a second set of commands from the descriptor table;